AMENDMENTS TO THE SPECIFICATION

Please replace the last paragraph of page 1 with the following amended paragraph:

The recent definition of the multiplexing principles and bitrates of an Optical Transport Network (ITU-T G.709) introduces a three level hierarchy with bitrates of ~~2,7~~ 2.7 Gbit/s, ~~10,7~~ 10.7 Gbit/s and 43 Gbit/s. Therefore, equipment is required for electrically processing these high bitrate signals. In particular, one issue in question is the internal signal distribution over backplanes and electrical cables which may distort internal electrical signals.

Please replace the first paragraph of the Detailed Description of the Invention on page 3 with the following amended paragraph:

The electrical signal regenerator 1 shown in figure 1 contains an equalizer 2, a clock data recovery circuit 3 (CDR in the following) coupled to the output of the equalizer, a switch 4 for selecting either the output ~~or~~ of the CDR circuit or via a bypass 24 the output of the equalizer. The selected signal from switch 4 is then fed to a decision circuit 5, i.e., a comparator which decides upon logical signal value 0 or 1 to produce output signal 7. Additionally, the signal regenerator has a loop back line 25 for test purposes.

Please replace the last paragraph of page 3 with the following amended paragraph:

A basic idea of the present invention is to adapt the operation of the signal regenerator to the bitrate of the received signal. The invention recognizes that for an electrical input signal 6

operating at ~~2,7~~ 2.7 Gbit/s, i.e., the lowest OTN bitrate, electrical equalization is sufficient, while for approximately 10 Gbit/s, additional CDR is necessary to improve the jitter properties of the signal regenerator. Therefore, the CDR circuit 3 contains a frequency meter which measures the frequency of the input signal 6 and controls the switch 4 to select either the output of the CDR circuit 3 or the output of the equalizer as output signal 7. The frequency meter is advantageously realized with an external quartz oscillator and a counter which counts the number of pulses of the recovered clock signal of the input signal per measurement cycle defined by the external oscillator.

Please replace the first paragraph of page 4 with the following amended paragraph:

It shall be noted that signals of the third OTN level, i.e., at 43 Gbit/s will not be discussed in the following as a bitrate of that level would encompass additional system limitations that shall not be discussed here and is not an object of the present invention. Typically, if 43 Gbit/s signals shall be processed electrically, one would choose a parallel format, e.g., converting the 43 Gbit/s into 4x~~10,75~~10.75 Gbit/s and process the 4 signals in parallel.

Please replace the third paragraph of page 5 with the following amended paragraph:

Via multiplier M20, the ~~ration~~ ratio between input and output of tap T1 is adjusted. This ~~ration~~ ratio depends on temperature and other external conditions. The control loop in tap T1 can thus be used to adapt the equalizer dynamically to changing conditions. However, it may also be sufficient to adjust tap T1 only once when switching the equalizer on and let the initial ~~ration~~ ratio fixed afterwards.

Please replace the third paragraph of page 5 with the following amended paragraph:

During start of the equalizer, a static signal is fed via test loop 21 to the input of the equalizer and amplifier OP20 turned off (i.e., no external input signal). Peak detector 10 measures the static test input and peak detector 11 measure~~d~~s the output of tap T1. The peak detectors are realized with a capacitor that is charged with the input signal until its voltage reaches the maximum signal amplitude after approximately ~~0,5~~0.5 µs. This peak measurement is cyclical, i.e., after a measurement cycle of about 2 µs, the voltage at the capacitor is reset to zero to start a new measurement cycle. Cyclical measurement is necessary to enable detection of a loss of the input signal, because if the peak detectors will not be reset, they would hold the maximum value, once fully charged, forever even when the input signal has long disappeared.

Please replace the first paragraph of page 6 with the following amended paragraph:

The results from the two peak detectors are fed via A/D-converter 12 to logic circuit 13, which is implemented with logic gates but could alternatively also be implemented with a processor and corresponding control software. The logic circuit 13 is a state machine that considers input and output peak values and determines according to a predefined optimization routine a scheduled value for the ratio. In the preferred embodiment, the scheduled ~~ration~~ ratio is ~~0,3~~0.3. When the equalizer is switched on, the logic circuit 13 adjusts the ~~ration~~ ratio between input and output of tap T1 in 10 steps. Afterwards, it may be disabled. Alternatively, it can continue to adjust the ~~ration~~ ratio to changing temperature conditions in an on-line tracking process. This may be advantageous, if the cooling of the entire signal regenerator is insufficient and therefore temperature will change during operation.

Please replace the second paragraph of page 6 with the following amended paragraph:

Peak detector 10 has thus two functions. On the one hand, it detects loss of input signal and raises via logic circuit 13 a corresponding alarm and on the other hand, it serves to measure and adjust the ~~ration~~ ratio between input and output of tap T1.

Please replace the last paragraph of page 6 with the following amended paragraph:

The equalizer 2 can compensate distortion of about 12 to 14 m coax cable or alternatively of about ~~1,7~~1.7 to ~~1,8~~1.8 m backplane. Figures ~~5a~~ 4a and ~~5b~~ 4b show signal measurements of a 10 Gbit/s signal after 104cm backplane plus 3m coax cable. Such measurements are typically referred to as eye diagrams. Figure ~~5a~~ 4a is an eye diagram of the distorted input signal. It can be observed that the eye is completely closed. Figure ~~5b~~ 4b shows the eye diagram after equalization. It can be observed that the eye has been widely opened by the equalizer. It can also be observed, however, that the poorly defined crossing area and the relatively soft rising edge would lead to jitter in the regenerated signal. Therefore, at 10 Gbit/s, additional CDR is required. Figure ~~5c~~ 4c shows the eye diagram after CDR. The signal is now perfectly re-shaped and does not show any jitter anymore.

Please replace the first paragraph of page 7 with the following amended paragraph:

The signal regenerator according to the present invention is adapted to compensate electrical cable distortion but can, however, also be used to compensate distortion of an optical signal due to dispersion effects. Figure ~~6~~ 5 shows the eye diagram of an optical signal after 1 km standard multi-mode fiber at the output from an optical receiver, i.e., directly after O/E conversion. No optical dispersion compensation has been applied. The eye diagram before equalization, i.e., the output signal from the optical receiver, has been nearly closed (upper part of the figure) and the equalizer perfectly opens the eye (lower part of the figure).

Please replace the second paragraph of page 7 with the following amended paragraph:

The test loop via OP21 described above can advantageously also be used for testing the equalizer during manufacturing on the wafer or after packaging. As the entire equalizer circuit is an ~~analogous~~ analog circuit without any logical components such as flip-flops in the signal path, looping back the inverted output to the input creates a ring oscillator. In particular, a first ring oscillator leads via tap T1 and a second ring oscillator leads via tap T2. Each ring oscillator oscillates at a different frequency. The difference of the two frequencies from these two paths gives an exact measure for the delay of the first tap T1. This can be used as a criterion to sort the chips during manufacturing, because the delay determines the maximum value frequency in the frequency response curve shown in figure 3. The tolerance for this frequency value is +/- 15%. Therefore, chips that have a deviation from the scheduled value of more than 15% will be sorted out.

Please replace the second paragraph of page 11 with the following amended paragraph:

In a further advantageous improvement, the 33th signal input in each switch module is used to generate a 4 GHz frequency signal. This can easily be achieved with the switching modules described below by simply switching a loop back in the test input port of each module. This results in a ring oscillation of 4 GHz, similar to the ring oscillation described above for test purposes of the equalizer. This 4 GHz signal is used as a monitor signal and switched to any un-used output port of the module, i.e., to each output port that carries no signal at the moment. The electrical signal regenerator connected to an un-used output in front of the subsequent switch module will automatically detect the 4 GHz tone rather than a ~~2,7~~ 2.7 Gbit/s signal or a ~~10,7~~ 10.7 Gbit/s and would thus know that the internal cable connection is alright. Conversely, if a regenerator does not detect neither a 4 GHz tone nor a valid ~~2,7~~ 1.7 or ~~10,7~~ 10.7 Gbit/s signal, it concludes that an internal cable is broken or disconnected and raises a corresponding alarm. The 4 GHz tone is thus used to continuously check internal matrix cabling that carry no signals at the moment. This improves reliability of the entire optical switch.